

1 **In the Claims**

2 Claims 1-47 were originally filed.

3 Claims 1-7, 27, 28, 37, and 38 have been previously cancelled without
4 prejudice.

5 Claim 39 has been previously amended.

6 Claim 33 is cancelled without prejudice.

7 Claims 34-36 are amended.

8 Accordingly, claims 8-26, 29-32, 34-36 and 39-47 are pending.

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10 **Clean Version Of The Pending Claims Under 37 C.F.R § 1.121(c)(3)**

11 **8.** An apparatus comprising:

12 a first XOR circuit having a first input to receive first data in a first format,
13 a second input to receive a periodic signal other than the first data; and an output
14 to provide the first data in a second format; and

15 a second XOR circuit having a first input coupled to the output of the first
16 XOR circuit, a second input coupled to receive the periodic signal other than the
17 first data, and an output to provide the first data in the first format.

18
19 **9.** The apparatus of claim 8, further comprising a memory for storing
20 the first data in the second format.

21
22 **10.** The apparatus of claim 9, wherein the periodic signal comprises an
23 address signal for addressing the memory.

D²

1 **11.** The apparatus of claim 10, wherein the address signal is generated
2 by a burst counter.

3
4 **12.** The apparatus of claim 8, further comprising:
5 a plurality of memories for storing the first data in the second format;
6 a burst counter for generating addresses for storing the first data in the first
7 format, wherein the periodic signal is derived from the addresses, wherein the first
8 XOR circuit, the second XOR circuit, and the burst counter reside on a buffer
9 chip.

10
11 **13.** The apparatus of claim 8, wherein the second format is different
12 from the first format.

13
14 **14.** The apparatus of claim 8, further comprising:
15 a first buffer coupled to the output of the first XOR circuit and to the first
16 input of the second XOR circuit;
17 a second buffer coupled to the output of the second XOR circuit.

18
19 **15.** An apparatus comprising:
20 a first circuit having a plurality of terminals;
21 a first plurality of XOR circuits each having a first input coupled to one of
22 the plurality of terminals, a second input coupled to receive a first periodic signal,
23 and an output; and
24 a second circuit having a first plurality of terminals each coupled to an
25 output of one of the first plurality of XOR circuits, and a second plurality of

1 terminals, wherein a number of the first plurality of terminals is different than a
2 number of second plurality of terminals.

3
4 **16.** The apparatus of claim 15, wherein the second circuit comprises a
5 serializer.

6
7 **17.** The apparatus of claim 16, wherein the serializer circuit comprises a
8 shift register.

9
10 **18.** The apparatus of claim 15, further comprising:
11 a second plurality of XOR circuits each having a first input coupled to one
12 of the first plurality of terminals of the second circuit, a second input coupled to
13 receive the first periodic signal, and an output coupled to one of the plurality of
14 terminals of the first circuit.

15
16 **19.** The apparatus of claim 18, wherein the second circuit comprises a
17 deserializer.

18
19 **20.** The apparatus of claim 19, wherein the deserializer circuit comprises
20 a shift register.

21
22 **21.** The apparatus of claim 18 further comprising:
23 a second plurality of XOR circuits each having a first input coupled to one
24 of the second plurality of terminals of the second circuit, a second input coupled to
25 a second periodic signal, and an output.

1
2 **22.** The apparatus of claim 21, wherein the first inputs of the first
3 plurality of XOR circuits are each coupled to the first circuit to receive first data in
4 a first format at a first data rate of the first periodic signal, and the outputs of the
5 first plurality of XOR circuits are structured to provide the first data in a second
6 format to the second circuit, and wherein the first inputs of the second plurality of
7 XOR circuits are each coupled to the second circuit to receive the first data in the
8 second format at a second data rate of the second periodic signal, and the outputs
9 of the second plurality of XOR circuits are structured to output the first data in a
10 third format.

11
12 **23.** The apparatus of claim 22, wherein the first data rate of the first
13 periodic signal is an integer multiple of the second data rate of the second periodic
14 signal.

15
16 **24.** The apparatus of claim 22, wherein the first circuit comprises a
17 memory for storing the first data, and wherein the first periodic signal comprises a
18 first address signal for addressing the memory, and the second periodic signal
19 comprises a second address signal for addressing the memory.

20
21 **25.** A system comprising:
22 a first device comprising:
23 a first circuit;

1 a first plurality of XOR circuits having first inputs coupled to receive
2 first data from the first circuit, second inputs each coupled to receive a bit of a first
3 predetermined number, and outputs; and

4 a second device comprising:

5 a second plurality of XOR circuits having first inputs coupled to the
6 outputs of the first plurality of XOR circuits, and second inputs coupled to receive
7 one bit of the first predetermined number.

8
9 **26.** The system of claim 25 wherein the first device further comprises:
10 a second circuit for storing the first predetermined number.

11
12 **29.** The system of claim 25, wherein the first predetermined number
13 comprises only one bit.

14
15 **30.** The system of claim 25, wherein:
16 the second device further comprises a third plurality of XOR circuits
17 having first inputs to receive second data, second inputs each coupled to receive a
18 bit of a second predetermined number, and outputs; and

19 the first device further comprises a fourth plurality of XOR circuits having
20 first inputs coupled to the outputs of the third plurality of XOR circuits, second
21 inputs each coupled to receive a bit of the second predetermined number, and
22 outputs coupled to the first circuit.

23
24 **31.** The system of claim 30, wherein the first predetermined number and
25 the second predetermined number are the same number.

1
2 **32.** The system of claim 30, wherein the second predetermined number
3 is only one bit.

4
5 **34.** (Once Amended) An apparatus comprising:
6 a first circuit;
7 a first plurality of XOR circuits having first inputs coupled to receive first
8 data from the first circuit, second inputs each coupled to receive a bit of a
9 predetermined number;
10 a second circuit providing the first predetermined number to the first
11 plurality of XOR circuits; and
12 a second plurality of XOR circuits having first inputs coupled to outputs of
13 the first plurality of XOR circuits, second inputs coupled to the predetermined
14 number, and outputs coupled to the first circuit.

15
16 **35.** (Once Amended) The apparatus of claim 3[3]4, wherein the
17 predetermined number is only one bit.

18
19 **36.** (Once Amended) The apparatus of claim 3[3]4, wherein the second
20 circuit comprises a pseudo-random number generator.

21
22 **39.** (Once Amended) A method of accessing a memory device
23 comprising:

24 writing data to the memory device via a first XOR circuit clocked by a
25 periodic signal other than a data signal.

1
2 **40.** A method of accessing a memory device comprising:
3 writing data to the memory device via first XOR circuit clocked by a
4 periodic signal other than the data; and
5 reading the data from the memory device via a second XOR circuit clocked
6 by the periodic signal.

7
8 **41.** A method of accessing a memory device comprising:
9 providing first data to a bus interface of the memory device in a first format
10 and at a first data rate;
11 reformatting the first data to a second format in response to an address
12 signal, the second format having a second data rate different than the first data
13 rate; and
14 storing the first data in the memory device in the second format.

15
16 **42.** The method of claim 41, wherein the step of storing the first data
17 comprises storing uncomplemented first data at even addresses, and storing
18 complemented first data at odd addresses of the memory device.

19
20 **43.** The method of claim 41, further comprising:
21 reformatting the stored first data into the first format; and
22 outputting the first data in the first format from the bus interface.

23
24 **44.** A memory device for interfacing with a data bus and an address bus,
25 the memory device comprising:

1 a reformatting circuit receiving data in a first format at a first data rate from
2 the data bus, and reformatting the data to a second format in response to an
3 address signal on the address bus that alternates the first data rate, the reformatted
4 data having a second data rate that is different than the first data rate; and

5 a memory circuit coupled to the reformatting circuit and storing the
6 reformatted data.

7
8 **45.** The memory device of claim 44, wherein the reformatting circuit
9 comprises an exclusive-OR circuit having a first input coupled to the data bus, a
10 second input coupled to the address signal, and an output coupled to the memory
11 circuit.

12
13 **46.** The memory circuit of claim 44, wherein the reformatting circuit
14 reformats the reformatted data in response to the address signal to regenerate the
15 data having the first format and the first data rate.

16
17 **47.** The memory circuit of claim 46, wherein the reformatting circuit
18 comprises an exclusive-OR (XOR) circuit having a first input coupled to the
19 memory circuit, a second input coupled to the address signal, and an output
20 coupled to the data bus.

21
22 **In the Drawings**

23 In Fig. 15 replace "1218" with "1216".
24

25 **REMARKS**